MACHINE TRANSLATION OF REFERENCE 2:

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CLAIMS

[Claim(s)]

[Claim 1]It is a signal transmission circuit where it comprises two or more unit circuits, and pulse voltage is outputted one by one from said unit circuit according to a drive pulse, A signal transmission circuit, wherein pulse voltage common to a gate of a discharge transistor which discharges an electric charge of both ends of bootstrap capacity established in said unit circuit is impressed.

[Claim 2]A signal transmission circuit where it comprises two or more unit circuits, and pulse voltage is outputted one by one from said unit circuit according to a drive pulse, comprising:

An output transistor which said unit circuit inputs said drive pulse into a drain, and is outputted from sauce as said pulse voltage.

Bootstrap capacity connected between a gate of said output transistor, and sauce.

A charging transistor to which sauce was connected at a gate of said output transistor in order to charge said bootstrap capacity.

A transistor for malfunction prevention which a drain was connected to a gate of

said output transistor, and was connected to an output driven by sauce or a source mode output of an output transistor in unit circuit where a gate is another.

[Claim 3]A signal transmission circuit where it comprises two or more unit circuits, and pulse voltage is outputted one by one from said unit circuit according to a drive pulse, comprising:

The 1st output transistor that said unit circuit inputs said drive pulse into a drain, and is outputted from sauce as said pulse voltage.

The 1st bootstrap capacity connected between a gate of said 1st output transistor, and sauce.

A charging transistor by which sauce was connected to a gate of said 1st output transistor, and a drain was connected to a power source wire, an earthing conductor, or a charge pulse line in order to charge said 1st bootstrap capacity.

The 2nd bootstrap capacity with which an end was connected to a gate of said charging transistor.

[Claim 4]A signal transmission circuit where it comprises two or more unit circuits, and pulse voltage is outputted one by one from said unit circuit according to a

drive pulse, comprising:

The 1st output transistor that said unit circuit inputs said drive pulse into a drain, and is outputted from sauce as said pulse voltage.

The 1st bootstrap capacity connected between a gate of said 1st output transistor, and sauce.

The 1st charging transistor by which sauce was connected to a gate of said 1st output transistor, and a drain was connected to a power source wire, an earthing conductor, or the 1st charge pulse line in order to charge said 1st bootstrap capacity.

The 2nd bootstrap capacity that one end was connected to a gate of said 1st charging transistor, and was connected to an output to which the other end was driven by the 2nd sauce or source mode output of an output transistor, Sauce is connected to an end of said 2nd bootstrap capacity in order to charge said 2nd bootstrap capacity, The 2nd charging transistor that a drain was connected to a power source wire, an earthing conductor, or the 2nd charge pulse line, and was connected to an output to which a gate was driven by the 3rd sauce or source mode output of an output transistor.

[Claim 5]The signal transmission circuit comprising according to claim 4:

The 1st discharge transistor by which a drain was connected to sauce of said 1st charging transistor in said signal transmission circuit.

The 2nd discharge transistor by which a drain was connected to sauce of said 2nd charging transistor.

[Claim 6]The signal transmission circuit comprising according to claim 5:

The 3rd discharge transistor connected to a terminal in which said signal transmission circuit differs from a terminal to which said 1st discharge transistor of said 1st bootstrap capacity was connected.

The 4th discharge transistor connected to a different terminal from a terminal to which said 2nd discharge transistor of said 2nd bootstrap capacity was connected.

[Claim 7]The signal transmission circuit according to claim 6, wherein said 3rd discharge transistor and said 4th discharge transistor are the same transistors.

[Claim 8]The signal transmission circuit according to claim 6 or 7 characterized by inputting said drive pulse at a gate of the said 3rd and 4th discharge

transistors.

[Claim 9]A signal transmission circuit of eight given in any 1 paragraph from claim 6, wherein an output driven by sauce or a source mode output of said 1st output transistor is supplied to a gate of said 2nd discharge transistor and the 3rd discharge transistor of the preceding paragraph.

[Claim 10]A signal transmission circuit of nine given in any 1 paragraph from claim 4, wherein said 2nd output transistor is an output transistor in a unit circuit of the preceding paragraph and said 3rd output transistor is an output transistor in a unit circuit of a beforehand stage.

[Claim 11]A signal transmission circuit of ten given in any 1 paragraph from claim 3, wherein said signal transmission circuit equips a gate of said 1st output transistor with a transistor for malfunction prevention to which a drain was connected.

[Claim 12]In said signal transmission circuit, a drain is connected to a gate of said 1st output transistor, A signal transmission circuit of ten given in any 1 paragraph from claim 3, wherein a gate is provided with a transistor for malfunction prevention connected to an output driven by sauce or a source mode output of an output transistor in a unit circuit of a beforehand stage.

[Claim 13]A period when pulse voltage is outputted from sauce of said 1st output transistor in a certain stage, A signal transmission circuit of 12 given in any 1 paragraph from claim 3, wherein a power-supply-voltage pulse which enables operation of said 1st charging transistor of the next step, and makes said 1st charging transistor of a stage prohibition of operation one after another is supplied to a drain of said 1st charging transistor.

[Claim 14]The signal transmission circuit according to claim 11 or 12 where conductance of said 1st charging transistor is characterized by being smaller than conductance of said transistor for malfunction prevention.

[Claim 15]Said all transistors are NMOS transistors and voltage lower than threshold voltage of said 1st output transistor is supplied to sauce of said 1st discharge transistor, A signal transmission circuit of 14 given in any 1 paragraph from claim 5, wherein voltage lower than threshold voltage of said 1st charging transistor is supplied to sauce of said 2nd discharge transistor.

[Claim 16]A signal transmission circuit of 14 given in any 1 paragraph from claim 6 which said all transistors are NMOS transistors and is characterized by supplying voltage lower than threshold voltage of the 2nd charging transistor of the next step to sauce of said 4th discharge transistor.

[Claim 17]The signal transmission circuit according to claim 11 or 12 which said all transistors are NMOS transistors and is characterized by supplying ground voltage to sauce of said transistor for malfunction prevention.

[Claim 18]The signal transmission circuit according to claim 10 or 11 which said all transistors are NMOS transistors and is characterized by supplying voltage lower than threshold voltage of said 1st output transistor to sauce of said transistor for malfunction prevention.

[Claim 19]Said all transistors are PMOS transistors and voltage higher than threshold voltage of said 1st output transistor is supplied to sauce of said 1st discharge transistor, A signal transmission circuit of 14 given in any 1 paragraph from claim 5, wherein voltage higher than threshold voltage of said 1st charging transistor is supplied to sauce of said 2nd discharge transistor.

[Claim 20]A signal transmission circuit of 14 given in any 1 paragraph from claim 6 which said all transistors are PMOS transistors and is characterized by supplying voltage higher than threshold voltage of the 2nd charging transistor of the next step to sauce of said 4th discharge transistor.

[Claim 21]The signal transmission circuit according to claim 11 or 12 which said all transistors are PMOS transistors and is characterized by supplying power

supply voltage to sauce of said transistor for malfunction prevention.

[Claim 22]The signal transmission circuit according to claim 11 or 12 which said all transistors are PMOS transistors and is characterized by supplying voltage higher than threshold voltage of said 1st output transistor to sauce of said transistor for malfunction prevention.

[Claim 23]A solid state camera provided with the signal transmission circuit according to claim 3 or 4.

[Claim 24]A camera carrying the solid state camera according to claim 23.

[Claim 25]A display provided with the signal transmission circuit according to claim 3 or 4.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention is applied to the shift register for driving an MOS image sensor, a camera, a display, etc., and relates to the signal transmission circuit which can be driven by the low voltage.

[0002]

[Description of the Prior Art]Drawing 4 is a circuit diagram showing the example of 1 composition of the conventional signal transmission circuit. Only many three-step portions are shown in drawing 4 among stage constitution on [of explanation] expedient. This signal transmission circuit The output transistor T12 to the next step, T22, and T32, The bootstrap capacity C11, C21, C31, and the charging transistor T11 and T21 which charge bootstrap capacity, and T31, It comprises the discharge transistor T13, T14, T23, T24, T33, and T34, and the power supply voltage VDD, the drive pulse V1, V2, and the start pulse VST are supplied.

[0003]Next, operation of the conventional signal transmission circuit constituted in this way is explained.

[0004]If the start pulse VST is set to a logic "High" level, the charging transistor T11 of the first rank will be turned on, One [the output transistor T12 of the first rank] if the bootstrap capacity C11 is charged to the power supply voltage VDD and the charge voltages of the bootstrap capacity C11 exceed the threshold voltage level of the output transistor T12.

[0005]Then, when the drive pulse V1 of a logic "High" level inputs into the drain

of the output transistor T12, in the gate of the output transistor T12. If the voltage of the drive pulse V1 and the potential difference of bootstrap capacity C11 both ends will be added and impressed and the gate potential of the output transistor T12 rises rather than the potential of the drive pulse V1, the drive pulse V1 will be used as output pulse OUT1 from the node N12.

[0006]The voltage of the node N12 is simultaneously impressed to the gate of the 2nd step of charging transistor T21, One [the 2nd step of output transistor T22] if the transistor T21 is turned on, the bootstrap capacity C21 is charged to the power supply voltage VDD and the charge voltages of the bootstrap capacity C21 exceed the threshold voltage level of the output transistor T22.

[0007]Then, when the drive pulse V2 of a logic "High" level inputs into the drain of the output transistor T22, in the gate of the output transistor T22. If the potential of the drive pulse V2 and the potential difference of the both ends of the bootstrap capacity C21 will be added and impressed and the gate potential of the output transistor T22 rises rather than the potential of the drive pulse V2, the drive pulse V2 will be used as output pulse OUT2 from the node N22.

[0008]The voltage of the node N22 is simultaneously impressed to the gate of the 3rd step of charging transistor T31, One [the 3rd step of output transistor

T22] if the charging transistor T31 is turned on, the bootstrap capacity C31 is charged to the power supply voltage VDD and the charge voltages of the bootstrap capacity C31 exceed the threshold voltage level of the output transistor T32.

[0009]By such operation being repeated, a signal transmission circuit will output the output after the output pulse OUT3 one by one further.

[0010]

[Problem(s) to be Solved by the Invention]The problem of the above-mentioned conventional signal transmission circuit is explained with reference to drawing 5.

[0011]Drawing 5 is a timing chart which shows the pulse voltage of each part in the conventional signal transmission circuit which used only NMOS. This circuit is a circuit of 5V system, and shows the case where the drive pulse V1, the voltage swing of V2, and the power supply voltage VDD are 5V.

[0012]In drawing 5, in the time t0, if the start pulse VST rises to 5V, the charging transistor T11 of the first rank is turned on, and the bootstrap capacity C11 is charged toward 5V which is the power supply voltage VDD, but. When the charging transistor T11 is NMOS of an enhancement type here, One [voltage VN11 of the node N11 to which the gate of the output transistor T12 was

connected under the influence of the threshold voltage Vt of the transistor T11 / only deltaH0 becomes low voltage (5 V-delta H0) from 5V which is the power supply voltage VDD, and / this state / the output transistor T12].

[0013]Next, when the drive pulse V1 of 5V inputs into the drain of the output transistor T12, in the time t1 in the gate (node N11) of the output transistor T12. Voltage HB 1 to which the voltage 5V of the drive pulse V1 and the potential difference (5 V-delta H0) of the both ends of the bootstrap capacity C11 were added will be impressed, and the pulse of the amplitude H1 will be outputted from the node N12.

[0014]Although the pulse voltage of the amplitude H1 of the node N12 is impressed to the gate of the 2nd step of charging transistor T21 and the charging transistor T21 is turned on simultaneously, The voltage of the node N21 to which the gate of the output transistor T22 was connected turns into voltage (H1-deltaH1) only with low deltaH1 from the voltage H1, and the bootstrap capacity C21 will be charged by the influence of threshold voltage VT of the transistor T21 to voltage (H1-deltaH1).

[0015]Similarly, also in time t2 and t3, operation of the time t1 will be repeated.

[0016]Thus, since only the voltage below 5V is added to the gate of a charging

transistor at the maximum in the case of the conventional signal transmission circuit, the bootstrap capacity can charge only voltage lower than 5V which is the power supply voltage VDD. The node N21 and the voltage of N31 descend gradually, and it becomes impossible therefore, for a signal transmission circuit to generate an output pulse at several steps or the point.

[0017]Operation will become more difficult if it becomes the voltage lowering of the electrical power system of a circuit, for example, the circuit of 3V system, etc., especially.

[0018]this invention is made in view of the above-mentioned problem, and comes out. The purpose Improvement in the speed or the signal transmission circuit which stable operation was possible even if it carried out voltage lowering, and was suitable for improvement in the speed or low power consumption, And it is in providing the camera carrying the solid state camera with which this signal transmission circuit is applied, and this solid state camera, and the display in which the above-mentioned signal transmission circuit is applied.

[0019]

[Means for Solving the Problem]In order to attain the aforementioned purpose,

the 1st signal transmission circuit concerning this invention, It is a signal transmission circuit where it comprises two or more unit circuits, and pulse voltage is outputted one by one from said unit circuit according to a drive pulse, Pulse voltage common to a gate of a discharge transistor for discharging an electric charge of both ends of bootstrap capacity established in said unit circuit is impressed.

[0020]According to this composition, even if an electric charge of both ends of bootstrap capacity can be discharged simultaneously at high speed and it accelerates a circuit power source, stable operation is possible, and a signal transmission circuit suitable for improvement in the speed can be realized.

[0021]The 2nd signal transmission circuit that this invention requires for this invention in order to attain the aforementioned purpose comprises two or more unit circuits, and is characterized by that a signal transmission circuit where pulse voltage is outputted one by one from a unit circuit according to a drive pulse comprises the following.

An output transistor which a unit circuit inputs a drive pulse into a drain, and is outputted from sauce as pulse voltage.

Bootstrap capacity connected between a gate of an output transistor, and sauce.

A charging transistor by which sauce was connected to a gate of an output transistor and a drain was connected to a power source wire, an earthing conductor, or a charge pulse line in order to charge bootstrap capacity.

A transistor for malfunction prevention which a drain was connected to a gate of an output transistor and connected to an output driven by sauce or a source mode output of an output transistor in unit circuit where a gate is another.

[0022]Between bootstrap capacity of a unit circuit and charging transistors is made into the 0V neighborhood, and pulse voltage can be prevented from coming out from an output transistor of the unit circuit concerned according to this composition. By this, even when threshold voltage of an output transistor is low, malfunction can be prevented, and the wide range of threshold voltage can be taken.

[0023]The 3rd signal transmission circuit that this invention requires for this invention in order to attain the aforementioned purpose comprises two or more unit circuits, and is characterized by that a signal transmission circuit where pulse voltage is outputted one by one from said unit circuit according to a drive pulse comprises the following.

The 1st output transistor that a unit circuit inputs a drive pulse into a drain, and is outputted from sauce as pulse voltage.

The 1st bootstrap capacity connected between a gate of the 1st output transistor, and sauce.

A charging transistor by which sauce was connected to a gate of the 1st output transistor, and a drain was connected to a power source wire, an earthing conductor, or a charge pulse line in order to charge the 1st bootstrap capacity.

The 2nd bootstrap capacity with which an end was connected to a gate of a charging transistor.

[0024]The 4th signal transmission circuit that this invention requires for this invention in order to attain the aforementioned purpose comprises two or more unit circuits, and is characterized by that a signal transmission circuit where pulse voltage is outputted one by one from a unit circuit according to a drive pulse comprises the following.

The 1st output transistor that a unit circuit inputs a drive pulse into a drain, and is outputted from sauce as pulse voltage.

The 1st bootstrap capacity connected between a gate of the 1st output transistor,

and sauce.

The 1st charging transistor by which sauce was connected to a gate of the 1st output transistor, and a drain was connected to a power source wire, an earthing conductor, or the 1st charge pulse line in order to charge the 1st bootstrap capacity.

The 2nd bootstrap capacity that one end was connected to a gate of the 1st charging transistor, and was connected to an output to which the other end was driven by the 2nd sauce or source mode output of an output transistor, Sauce is connected to an end of the 2nd bootstrap capacity in order to charge the 2nd bootstrap capacity, The 2nd charging transistor that a drain was connected to a power source wire, an earthing conductor, or the 2nd charge pulse line, and was connected to an output to which a gate was driven by the 3rd sauce or source mode output of an output transistor.

[0025]According to this composition, first by a source mode output of the 3rd output transistor (for example, it can set to a unit circuit of a beforehand stage) being impressed to a gate of the 2nd charging transistor. By the 2nd bootstrap capacity being charged, one end of the 2nd bootstrap capacity being connected

to a gate of the 1st charging transistor, and an output of the 2nd output transistor (for example, it can set to a unit circuit of the preceding paragraph) being applied to the other end. Voltage higher than before will be added to a gate of the 1st charging transistor, and gate potential of the 1st charging transistor can be made higher than the power supply voltage VDD. Thereby, the 1st bootstrap capacity can be charged at the power supply voltage VDD, and descent of charge voltages to the 1st bootstrap capacity can be prevented. Therefore, when a transmission number of stages increases, it can prevent that output pulse voltage does not decline gradually or an output pulse stops coming out at several steps or the point.

[0026]As for the 4th signal transmission circuit, it is preferred to have the 1st discharge transistor by which a drain was connected to sauce of the 1st charging transistor, and the 2nd discharge transistor by which a drain was connected to sauce of the 2nd charging transistor.

[0027]The 3rd discharge transistor connected to a terminal in which the 4th signal transmission circuit differs from a terminal to which the 1st discharge transistor of the 1st bootstrap capacity was connected, It is preferred to have the 4th discharge transistor connected to a different terminal from a terminal to

which said 2nd discharge transistor of the 2nd bootstrap capacity was connected.

[0028]In this case, it is preferred that the 3rd discharge transistor and the 4th discharge transistor are the same transistors.

[0029]In a gate of the 3rd and 4th discharge transistors, it is preferred that a drive pulse is inputted. Thereby, it can discharge by being stabilized by a direct-drive pulse being added.

[0030]It is preferred that an output driven by the 1st source voltage or source voltage of an output transistor is supplied to a gate of the 2nd discharge transistor and the 3rd discharge transistor of the preceding paragraph. Thereby, the 2nd bootstrap capacity and the 1st bootstrap capacity of the preceding paragraph can be discharged simultaneously.

[0031]Thus, only by adding four discharge transistors, discharge of bootstrap capacity can be performed and this invention can be applied also to small circuitry of a scale without other external input pulses.

[0032]In the 4th signal transmission circuit, the 2nd output transistor is an output transistor in a unit circuit of the preceding paragraph, and, as for the 3rd output transistor, it is preferred that it is an output transistor in a unit circuit of a beforehand stage.

[0033]According to this composition, by using an output of a shift register, an excessive pulse added to a gate of a charging transistor can be omitted, and circuit structure can be made small.

[0034]As for the 3rd and 4th signal transmission circuits, it is preferred that a drain is provided with a transistor for malfunction prevention connected to a gate of the 1st output transistor.

[0035]According to this composition, even when threshold voltage of an output transistor is low, malfunction can be prevented, and the wide range of threshold voltage can be taken.

[0036]As for the 3rd and 4th signal transmission circuits, it is preferred to have a transistor for malfunction prevention by which a drain was connected to a gate of the 1st output transistor, and a gate was connected to sauce of an output transistor of a beforehand stage.

[0037]According to this composition, this invention is applicable also to small circuitry of a scale without other external input pulses with having constituted so that sauce of an output transistor of a beforehand stage might be connected to a gate of a transistor for malfunction prevention.

[0038]In the 3rd and 4th signal transmission circuits, it is preferred that a

power-supply-voltage pulse which enables operation of a charging transistor of a period when pulse voltage is outputted to sauce of an output transistor of a certain stage, and the next step, and makes one charging transistor of a stage after another prohibition of operation is supplied to a drain. For example, when a charging transistor consists of NMOSes, as a power-supply-voltage pulse, "High" level voltage is supplied to a drain of a charging transistor of the next step, and "Low" level voltage is supplied to a drain of a charging transistor of a stage one after another. When a charging transistor consists of PMOSes, as a power-supply-voltage pulse, "Low" level voltage is supplied to a drain of a charging transistor of the next step, and "High" level voltage is supplied to a drain of a charging transistor of a stage one after another.

[0039]According to this composition, a transistor for malfunction prevention can be omitted and circuit structure can be reduced.

[0040]Or it is preferred that conductance of the 1st charging transistor is smaller than conductance of a transistor for malfunction prevention.

[0041]According to this composition, the positive terminal side of the 1st bootstrap capacity can be brought more close to 0V, and malfunction can be prevented more certainly.

[0042]In the 3rd and 4th signal transmission circuits, when all transistors are NMOS transistors, earth potentials are supplied to at least one of sauce of the 1st to 4th discharge transistor, and sauce of a transistor for malfunction prevention.

[0043]Or when all transistors are NMOS transistors in the 3rd and 4th signal transmission circuits, To at least one of sauce of the 1st to 4th discharge transistor, and sauce of a transistor for malfunction prevention, voltage lower than threshold voltage of the 1st output transistor is supplied.

[0044]In the 3rd and 4th signal transmission circuits, when all transistors are PMOS transistors, power supply voltage is supplied to at least one of sauce of the 1st to 4th discharge transistor, and sauce of a transistor for malfunction prevention.

[0045]Or when all transistors are PMOS transistors in the 3rd and 4th signal transmission circuits, To at least one of sauce of the 1st to 4th discharge transistor, and sauce of a transistor for malfunction prevention, voltage higher than threshold voltage of the 1st output transistor is supplied.

[0046]By the above-mentioned composition, a charging transistor or an output transistor is stabilized and a state of OFF can be maintained.

[0047]In order to attain the aforementioned purpose, a solid state camera concerning this invention was provided with the 3rd or 4th signal transmission circuit.

[0048]In order to attain the aforementioned purpose, a camera concerning this invention carried a solid state camera concerning this invention.

[0049]In order to attain the aforementioned purpose, a display concerning this invention was provided with the 3rd or 4th signal transmission circuit.

[0050]According to the above-mentioned composition, an effect can be demonstrated in a solid state camera and a camera which carries it which can guarantee stable operation even if it carries out voltage lowering of the circuit power source, and are applied to a portable equipment which needs to attain especially low power consumption, and a liquid crystal display.

[0051]

[Embodiment of the Invention]Hereafter, the suitable embodiment of this invention is described with reference to drawings.

[0052](A 1st embodiment) Drawing 1 is a circuit diagram showing the example of 1 composition of the signal transmission circuit concerning a 1st embodiment of this invention. The gate of the discharge transistor of the preceding paragraph is

connected common to the sauce of the output transistor of the next step, and the point that this embodiment differs from the conventional example shown in drawing 4 is one of the points that common output pulse voltage is impressed. About other composition, it is the same as the conventional example of drawing 5, and the same numerals are attached in drawing 1.

[0053]In drawing 1, if the start pulse VST is set to a logic "High" level, The 1st charging transistor T11 that charges the 1st bootstrap capacity C11 in the first rank is turned on, One [the output transistor T12 of the first rank] if the 1st bootstrap capacity C11 is charged with the power supply voltage VDD and the charge voltages of the 1st bootstrap capacity C11 exceed the threshold voltage level of the output transistor T12.

[0054]Then, when the drive pulse V1 of a logic "High" level inputs into the drain of the output transistor T12, in the gate of the output transistor T12. If the voltage of the drive pulse V1 and the potential difference of the 1st bootstrap capacity C11 both ends will be added and impressed and the gate potential of the output transistor T12 rises rather than the potential of the drive pulse V1, The drive pulse V1 is used as output pulse OUT1 from the output node N12 of the first rank.

[0055]Simultaneously, if the drive pulse V1 is outputted to the node N12, the 2nd

step of 1st charging transistor T21 by which the gate was connected to the node N12 will be turned on, One [the 2nd step of output transistor T22] if the 1st bootstrap capacity C21 is charged with the power supply voltage VDD and the charge voltages of the 1st bootstrap capacity C21 exceed the threshold voltage level of the output transistor T22.

[0056]Then, when the drive pulse V2 of a logic "High" level inputs into the drain of the output transistor T22, in the gate of the output transistor T22. If the potential of the drive pulse V2 and the potential difference of the 1st capacity C21 both ends for a bootstrap will be added and impressed and the gate potential of the output transistor T22 rises rather than the potential of the drive pulse V2, The drive pulse V2 is used as output pulse OUT2 from the 2nd step of output node N22.

[0057]Since this output pulse OUT2 is impressed common to the gate of the 1st discharge transistor T13 in the first rank, and the 2nd discharge transistor T14, When the drive pulse V2 is outputted to the 2nd step of output node N22, the electric charge of the 1st bootstrap capacity C11 both ends of the first rank will be discharged at high speed and simultaneous.

[0058]Even if the advantage of the signal transmission circuit by this

embodiment accelerates a circuit power source by discharging the electric charge of the both ends of the 1st bootstrap capacity C11 at high speed and simultaneous, stable operation is possible for it here, and a signal transmission circuit suitable for improvement in the speed can be realized.

[0059]Simultaneously, if the drive pulse V2 is outputted to the node N22, the 3rd step of 1st charging transistor T31 by which the gate was connected to the node N22 will be turned on, One [the 3rd step of output transistor T32] if the 1st bootstrap capacity C31 is charged with the power supply voltage VDD and the charge voltages of the 1st bootstrap capacity C31 exceed the threshold voltage level of the output transistor T32.

[0060]Then, when the drive pulse V1 of a logic "High" level inputs into the drain of the output transistor T32, in the gate of the output transistor T32. If the potential of the drive pulse V1 and the potential difference of the 1st capacity C31 both ends for a bootstrap will be added and impressed and the gate potential of the output transistor T32 rises rather than the potential of the drive pulse V1, The drive pulse V1 is used as output pulse OUT3 from the 3rd step of output node N32.

[0061]Since this output pulse OUT3 is impressed common to the gate of the 1st

discharge transistor T23 in the 2nd step, and the 2nd discharge transistor T24, When the drive pulse V1 is outputted to the 3rd step of output node N32, the electric charge of the 2nd step of 1st bootstrap capacity C21 both ends will be discharged at high speed and simultaneous.

[0062]By such operation being repeated, a signal transmission circuit will output an output pulse one by one further.

[0063]Although each sauce of the 1st and 2nd discharge transistors is made into earth potentials (0V), if each source voltage is a value smaller than the threshold voltage of an output transistor, the same effect will be acquired even if it is not 0V.

[0064](A 2nd embodiment) Drawing 2 is a circuit diagram showing the example of 1 composition of the signal transmission circuit concerning a 2nd embodiment of this invention. In the unit circuit after the 2nd step the point that this embodiment differs from a 1st embodiment, The 2nd bootstrap capacity (C22, C32) and the 2nd charging transistor (T25, T35) that charges the 2nd bootstrap capacity, In the 3rd discharge transistor (T26, T36) that discharges the electric charge of the both ends of the 2nd bootstrap capacity, and the unit circuit after the 3rd step, To the plus side edge child (node N31) of the 1st bootstrap capacity

(C31), a drain, A gate is connected to the output node (N12) of the beforehand stage, and the transistor for malfunction prevention (T38) with which sauce is grounded is added, The plus side edge child (the node N25, N35) of the 2nd bootstrap capacity is connected to the gate of the 1st charging transistor (T21, T31) in the own stage, It is in the point of having connected the minus side edge child (the node N12, N22) of the 2nd bootstrap capacity to the gate of the 2nd charging transistor (T25, T35) in the next step.

[0065]In drawing 2, if start pulse VST2 is set to a logic "High" level, The 1st charging transistor T11 that charges the 1st bootstrap capacity C11 in the first rank is turned on, One [the output transistor T12 of the first rank] if the 1st bootstrap capacity C11 is charged with the power supply voltage VDD and the charge voltages of the 1st bootstrap capacity C11 exceed the threshold voltage level of the output transistor T12.

[0066]If start pulse VST1 is set to a logic "High" level, the 2nd charging transistor T25 that charges the 2nd bootstrap capacity C22 in the 2nd step will be turned on, and the 2nd bootstrap capacity C22 will be charged with the power supply voltage VDD.

[0067]Then, when the drive pulse V1 of a logic "High" level inputs into the drain

of the output transistor T12, in the gate of the output transistor T12. If the voltage of the drive pulse V1 and the potential difference of the 1st bootstrap capacity C11 both ends will be added and impressed and the gate potential of the output transistor T12 rises rather than the potential of the drive pulse V1, The drive pulse V1 is used as output pulse OUT1 from the output node N12 of the first rank.

[0068]Here the advantage of the signal transmission circuit by this embodiment, In the gate of the 2nd step of 1st charging transistor T21 connected to the node N25 of the plus side edge child of the 2nd charged bootstrap capacity C22. The voltage of the drive pulse V1 and the potential difference of the 2nd bootstrap capacity C22 both ends which were outputted to the output node N12 will be added and impressed, Since it goes up rather than the power supply voltage VDD whose gate potential of the 1st charging transistor T21 is drain potential, it is in the point that the 2nd step of 1st bootstrap capacity C21 can be charged at the power supply voltage VDD.

[0069]By this, even if the 1st charging transistor T21 that charges the 2nd step of 1st capacity C21 for a bootstrap is NMOS of an enhancement type, The 1st bootstrap capacity C21 can be charged certainly at the power supply voltage VDD, and the output transistor T22 can be made one.

[0070]When the drive pulse V1 is outputted to the output node N12, simultaneously, and the 3rd step of 2nd bootstrap capacity C32 is charged. [the 3rd step of 2nd charging transistor T35 by which the gate was connected to the output node N12]

[0071]Then, when the drive pulse V2 of a logic "High" level inputs into the drain of the output transistor T22, in the gate of the output transistor T22. If the potential of the drive pulse V2 and the potential difference of the 1st bootstrap capacity C21 both ends will be added and impressed and the gate potential of the output transistor T22 rises rather than the potential of the drive pulse V2, The drive pulse V2 is used as output pulse OUT2 from the 2nd step of output node N22.

[0072]In the gate of the 3rd step of 1st charging transistor T31 simultaneously connected to the node N35 which is a plus side edge child of the 2nd bootstrap capacity C32. The voltage of the drive pulse V2 and the potential difference of the 2nd bootstrap capacity C32 both ends which were outputted to the output node N22 will be added and impressed, One [the 3rd step of 1st bootstrap capacity C31 is certainly charged by the power supply voltage VDD, and / the output transistor T32] since the gate potential of the 1st charging transistor T31

rises rather than the power supply voltage VDD which is drain potential.

[0073]By such operation being repeated, a signal transmission circuit will output the output pulse OUT3 or subsequent ones one by one further.

[0074]Thus, in all the signal-transmission stages, the 1st bootstrap capacity can charge the power supply voltage VDD certainly, and the signal transmission circuit which can generate the output pulse of the low voltage without a voltage drop can be realized.

[0075]In order to lessen the transistor and power supply of a circuit as a means to discharge the voltage which charged bootstrap capacity, in the case of the 1st bootstrap capacity C21 in the 2nd step, The drain of the 1st discharge transistor T23 is connected to the plus side edge child of the 1st bootstrap capacity C21, The drain of the 2nd discharge transistor T24 is connected to the minus side edge child of the 1st bootstrap capacity C21, The output node N32 connected to the sauce of the 3rd step of output transistor T32 which is the next step at the gate of the 1st discharge transistor T23 and the 2nd discharge transistor T24 is connected. By this, when the drive pulse V1 is outputted to the 3rd step of output node N32, the 1st bootstrap capacity C21 in the 2nd step will be discharged.

[0076]On the other hand, in the case of the 2nd bootstrap capacity C22 in the

2nd step, The output node N22 which connected the drain of the 3rd discharge transistor T26 to the plus side edge child of the 2nd bootstrap capacity C22, and was connected to the sauce of the 2nd step of output transistor T22 which is self at the gate of the 3rd discharge transistor T26 is connected. By this, when the drive pulse V2 is outputted to the 2nd step of output node N22, the 2nd bootstrap capacity C22 in the 2nd step will be discharged.

[0077]By this composition, only by adding three discharge transistors, the 1st and 2nd bootstrap capacity can be discharged and the small circuitry of a scale without other external input pulses can also realize the signal transmission circuit of this embodiment.

[0078]The drain was connected to the plus side edge child (node N31) of the 1st bootstrap capacity C31 in the 3rd step, the gate was connected to the output node N12 in the first rank, and the transistor T38 for malfunction prevention with which sauce was grounded is formed. One [the 1st charging transistor T31 / with the potential of the node N35 / some] when the 2nd bootstrap capacity C32 in the 3rd step is charged. And one [since the 1st bootstrap capacity C31 is charged somewhat] although the output transistors T32 are some when the threshold voltage of the output transistor T32 is low. When the drive pulse V1 is

outputted to the output node N12 of the first rank at this time, the drive pulse V1 may be simultaneously outputted also to the 3rd step of output node N32.

[0079]In order to prevent outputting the drive pulse V1 to the output node N32, When the transistor T38 for malfunction prevention is formed and the drive pulse V1 is outputted to the output node N12 of the first rank, the node N31 is made into the 0V neighborhood, and the drive pulse V1 is made not to be outputted to the 3rd step of output node N32. [the transistor T38 for malfunction prevention]

[0080]At this time, the conductance of the 1st charging transistor T31 in the 3rd step by making it smaller than the conductance of the transistor T38 for malfunction prevention. The positive terminal side of the 1st bootstrap capacity C31 can be brought more close to 0V, and malfunction can be prevented more certainly.

[0081]Thus, the transistor for malfunction prevention is provided in each stage after the 3rd step, and by impressing the output pulse of the beforehand stage to the gate of the transistor for malfunction prevention, even when the threshold voltage of an output transistor is low, malfunction can be prevented, and the wide range of threshold voltage can be taken.

[0082]With having constituted so that the sauce of the output transistor of the

beforehand stage might be connected to the gate of the transistor for malfunction prevention, even when it is small circuitry of a scale without other external input pulses, the signal transmission circuit by this embodiment can be realized.

[0083]Although each sauce of the discharge transistor and the transistor for malfunction prevention is made into earth potentials (0V), if each source voltage is a value smaller than the threshold voltage of an output transistor, the same effect will be acquired even if it is not 0V.

[0084]Since DC voltage is impressed to the drain of the 1st and 2nd charging transistors as the power supply voltage VDD, a possibility that malfunction will take place occurs in it, and it is necessary in it to include the transistor for malfunction prevention but, and. Malfunction can be prevented by impressing pulse voltage to the drain of a charging transistor as the power supply voltage VDD. That is, the drain of the charging transistor of the period and the next step which output voltage has generated in the sauce of an output transistor can be used as the "High" level, and the transistor for malfunction prevention can be omitted by using one drain of the charging transistor of the stage after another as the "Low" level.

[0085]Drawing 3 is a timing chart which shows the pulse voltage of each part in the signal transmission circuit of drawing 2 which used only NMOS. This circuit is a circuit of 3V system, and shows the case where the drive pulse V1, the voltage swing of V2, and the power supply voltage VDD are 3V. However, the voltage swing of start pulse VST2 sets the voltage swing of 5V and start pulse VST1 to 3V. Setting only the voltage swing of start pulse VST2 to 5V here, Since the high voltage from the preceding paragraph cannot be supplied only when it is the 1st charging transistor T11 of the first rank into which start pulse VST2 is inputted, When only start pulse VST2 drives the 1st charging transistor T11 by 5V [higher than 3V which is the drive pulse V1 and a voltage swing of V2], It is because the voltage drop by the 1st charging transistor T11 is prevented and charge of 3V which is the power supply voltage VDD of the 1st bootstrap capacity C11 is enabled.

[0086]In drawing 3, the voltage of start pulse VST2 rises to 5V in the time t0, One [the 1st bootstrap capacity C11 is charged via the transistor T11 by 3V which is the power supply voltage VDD, and / the output transistor T12] even when there is the threshold voltage Vt of the 1st charging transistor T11 that is NMOS of an enhancement type.

[0087]Simultaneously, the voltage of start pulse VST1 rises to 3V, and the 2nd bootstrap capacity C22 is charged via the 2nd charging transistor T25.

[0088]Next, when the drive pulse V1 rises to 3V and inputs into the drain of the output transistor T12 in the time t1, in the gate of the output transistor T12. Since voltage HB 1 high voltage to which the voltage 3V of the drive pulse V1 and the potential difference 3V of bootstrap capacity C11 both ends were added is impressed, the drive pulse V1 of 3V amplitude will be certainly outputted as output pulse OUT1 from the output node N12.

[0089]And one [high-tension HB 25 of the node N25 connected to the plus side edge child of the 2nd bootstrap capacity C22 is simultaneously inputted into the gate of the 1st charging transistor T21, and / the transistor T21], The 1st bootstrap capacity C21 will be charged by 3V which is the power supply voltage VDD certainly.

[0090]At this time, the voltage (3 V-delta H35) in which the node N35 is lower than 3V is charged, and the same voltage also as the gate of the 1st charging transistor T31 is impressed. In this case, so that the potential of the node N31 connected to the sauce of the 1st charging transistor T31 may not become more than the threshold voltage of the 1st charging transistor T31, By and bringing the

node N31 in the earth-potentials direction close, it can prevent outputting the drive pulse V1 to the node N32 at the time t1. [the malfunction prevention transistor T38]

[0091]Similarly, also in time t2 and t3, operation of the time t1 will be repeated.

[0092]As mentioned above, in order to add the plus side edge child voltage of the 2nd bootstrap capacity to the gate of the 1st charging transistor according to this embodiment, The signal transmission circuit which can generate the output pulse of the low voltage of 3V which can charge the 1st bootstrap capacity certainly at the power supply voltage 3V, and does not have a voltage drop is realizable.

[0093]In this embodiment, although the case of the NMOS transistor was illustrated and explained, the same effect can be acquired also about the case where it is a PMOS transistor altogether.

[0094]Amplitude can be enlarged for the source voltage of an output transistor using a drive circuit, and voltage can be increased in this embodiment.

[0095]

[Effect of the Invention]As explained above, according to this invention, the bootstrap capacity of the next step can be charged at the power supply voltage

VDD, and descent of the charge voltages to bootstrap capacity can be prevented. Therefore, when a transmission number of stages increases, it can prevent that output pulse voltage does not decline gradually or an output pulse stops coming out at several steps or the point. By this, the signal transmission circuit in which a stable low voltage drive is possible is realizable.

[0096]Meeting the request of low voltage drive realization of a liquid crystal display and an MOS type pickup device, this signal transmission circuit uses a signal transmission circuit for a shift register, considers voltage lowering as realization, and is very useful industrially.

TECHNICAL FIELD

[Field of the Invention]This invention is applied to the shift register for driving an MOS image sensor, a camera, a display, etc., and relates to the signal transmission circuit which can be driven by the low voltage.

PRIOR ART

[Description of the Prior Art]Drawing 4 is a circuit diagram showing the example of 1 composition of the conventional signal transmission circuit. Only many three-step portions are shown in drawing 4 among stage constitution on [of explanation] expedient. This signal transmission circuit The output transistor T12 to the next step, T22, and T32, The bootstrap capacity C11, C21, C31, and the charging transistor T11 and T21 which charge bootstrap capacity, and T31, It comprises the discharge transistor T13, T14, T23, T24, T33, and T34, and the power supply voltage VDD, the drive pulse V1, V2, and the start pulse VST are supplied.

[0003]Next, operation of the conventional signal transmission circuit constituted in this way is explained.

[0004]If the start pulse VST is set to a logic "High" level, the charging transistor T11 of the first rank will be turned on, One [the output transistor T12 of the first rank] if the bootstrap capacity C11 is charged to the power supply voltage VDD and the charge voltages of the bootstrap capacity C11 exceed the threshold voltage level of the output transistor T12.

[0005]Then, when the drive pulse V1 of a logic "High" level inputs into the drain of the output transistor T12, in the gate of the output transistor T12. If the voltage

of the drive pulse V1 and the potential difference of bootstrap capacity C11 both ends will be added and impressed and the gate potential of the output transistor T12 rises rather than the potential of the drive pulse V1, the drive pulse V1 will be used as output pulse OUT1 from the node N12.

[0006]The voltage of the node N12 is simultaneously impressed to the gate of the 2nd step of charging transistor T21, One [the 2nd step of output transistor T22] if the transistor T21 is turned on, the bootstrap capacity C21 is charged to the power supply voltage VDD and the charge voltages of the bootstrap capacity C21 exceed the threshold voltage level of the output transistor T22.

[0007]Then, when the drive pulse V2 of a logic "High" level inputs into the drain of the output transistor T22, in the gate of the output transistor T22. If the potential of the drive pulse V2 and the potential difference of the both ends of the bootstrap capacity C21 will be added and impressed and the gate potential of the output transistor T22 rises rather than the potential of the drive pulse V2, the drive pulse V2 will be used as output pulse OUT2 from the node N22.

[0008]The voltage of the node N22 is simultaneously impressed to the gate of the 3rd step of charging transistor T31, One [the 3rd step of output transistor T22] if the charging transistor T31 is turned on, the bootstrap capacity C31 is

charged to the power supply voltage VDD and the charge voltages of the bootstrap capacity C31 exceed the threshold voltage level of the output transistor T32.

[0009]By such operation being repeated, a signal transmission circuit will output the output after the output pulse OUT3 one by one further.

EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, according to this invention, the bootstrap capacity of the next step can be charged at the power supply voltage VDD, and descent of the charge voltages to bootstrap capacity can be prevented. Therefore, when a transmission number of stages increases, it can prevent that output pulse voltage does not decline gradually or an output pulse stops coming out at several steps or the point. By this, the signal transmission circuit in which a stable low voltage drive is possible is realizable.

[0096]Meeting the request of low voltage drive realization of a liquid crystal display and an MOS type pickup device, this signal transmission circuit uses a

signal transmission circuit for a shift register, considers voltage lowering as realization, and is very useful industrially.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]The problem of the above-mentioned conventional signal transmission circuit is explained with reference to drawing 5.

[0011]Drawing 5 is a timing chart which shows the pulse voltage of each part in the conventional signal transmission circuit which used only NMOS. This circuit is a circuit of 5V system, and shows the case where the drive pulse V1, the voltage swing of V2, and the power supply voltage VDD are 5V.

[0012]In drawing 5, in the time t0, if the start pulse VST rises to 5V, the charging transistor T11 of the first rank is turned on, and the bootstrap capacity C11 is charged toward 5V which is the power supply voltage VDD, but. When the charging transistor T11 is NMOS of an enhancement type here, One [voltage VN11 of the node N11 to which the gate of the output transistor T12 was connected under the influence of the threshold voltage Vt of the transistor T11 / only deltaH0 becomes low voltage (5 V-delta H0) from 5V which is the power

supply voltage VDD, and / this state / the output transistor T12].

[0013]Next, when the drive pulse V1 of 5V inputs into the drain of the output transistor T12, in the time t1 in the gate (node N11) of the output transistor T12. Voltage HB 1 to which the voltage 5V of the drive pulse V1 and the potential difference (5 V-delta H0) of the both ends of the bootstrap capacity C11 were added will be impressed, and the pulse of the amplitude H1 will be outputted from the node N12.

[0014]Although the pulse voltage of the amplitude H1 of the node N12 is impressed to the gate of the 2nd step of charging transistor T21 and the charging transistor T21 is turned on simultaneously, The voltage of the node N21 to which the gate of the output transistor T22 was connected turns into voltage (H1-deltaH1) only with low deltaH1 from the voltage H1, and the bootstrap capacity C21 will be charged by the influence of threshold voltage VT of the transistor T21 to voltage (H1-deltaH1).

[0015]Similarly, also in time t2 and t3, operation of the time t1 will be repeated.

[0016]Thus, since only the voltage below 5V is added to the gate of a charging transistor at the maximum in the case of the conventional signal transmission circuit, the bootstrap capacity can charge only voltage lower than 5V which is the

power supply voltage VDD. The node N21 and the voltage of N31 descend gradually, and it becomes impossible therefore, for a signal transmission circuit to generate an output pulse at several steps or the point.

[0017]Operation will become more difficult if it becomes the voltage lowering of the electrical power system of a circuit, for example, the circuit of 3V system, etc., especially.

[0018]this invention is made in view of the above-mentioned problem, and comes out. The purpose Improvement in the speed or the signal transmission circuit which stable operation was possible even if it carried out voltage lowering, and was suitable for improvement in the speed or low power consumption, And it is in providing the camera carrying the solid state camera with which this signal transmission circuit is applied, and this solid state camera, and the display in which the above-mentioned signal transmission circuit is applied.

MEANS

[Means for Solving the Problem]In order to attain the aforementioned purpose, the 1st signal transmission circuit concerning this invention, It is a signal

transmission circuit where it comprises two or more unit circuits, and pulse voltage is outputted one by one from said unit circuit according to a drive pulse, Pulse voltage common to a gate of a discharge transistor for discharging an electric charge of both ends of bootstrap capacity established in said unit circuit is impressed.

[0020]According to this composition, even if an electric charge of both ends of bootstrap capacity can be discharged simultaneously at high speed and it accelerates a circuit power source, stable operation is possible, and a signal transmission circuit suitable for improvement in the speed can be realized.

[0021]The 2nd signal transmission circuit that this invention requires for this invention in order to attain the aforementioned purpose comprises two or more unit circuits, and is characterized by that a signal transmission circuit where pulse voltage is outputted one by one from a unit circuit according to a drive pulse comprises the following.

An output transistor which a unit circuit inputs a drive pulse into a drain, and is outputted from sauce as pulse voltage.

Bootstrap capacity connected between a gate of an output transistor, and sauce.

A charging transistor by which sauce was connected to a gate of an output

transistor and a drain was connected to a power source wire, an earthing conductor, or a charge pulse line in order to charge bootstrap capacity.

A transistor for malfunction prevention which a drain was connected to a gate of an output transistor and connected to an output driven by sauce or a source mode output of an output transistor in unit circuit where a gate is another.

[0022]Between bootstrap capacity of a unit circuit and charging transistors is made into the 0V neighborhood, and pulse voltage can be prevented from coming out from an output transistor of the unit circuit concerned according to this composition. By this, even when threshold voltage of an output transistor is low, malfunction can be prevented, and the wide range of threshold voltage can be taken.

[0023]The 3rd signal transmission circuit that this invention requires for this invention in order to attain the aforementioned purpose comprises two or more unit circuits, and is characterized by that a signal transmission circuit where pulse voltage is outputted one by one from said unit circuit according to a drive pulse comprises the following.

The 1st output transistor that a unit circuit inputs a drive pulse into a drain, and is

outputted from sauce as pulse voltage.

The 1st bootstrap capacity connected between a gate of the 1st output transistor, and sauce.

A charging transistor by which sauce was connected to a gate of the 1st output transistor, and a drain was connected to a power source wire, an earthing conductor, or a charge pulse line in order to charge the 1st bootstrap capacity.

The 2nd bootstrap capacity with which an end was connected to a gate of a charging transistor.

[0024]The 4th signal transmission circuit that this invention requires for this invention in order to attain the aforementioned purpose comprises two or more unit circuits, and is characterized by that a signal transmission circuit where pulse voltage is outputted one by one from a unit circuit according to a drive pulse comprises the following.

The 1st output transistor that a unit circuit inputs a drive pulse into a drain, and is outputted from sauce as pulse voltage.

The 1st bootstrap capacity connected between a gate of the 1st output transistor, and sauce.

The 1st charging transistor by which sauce was connected to a gate of the 1st output transistor, and a drain was connected to a power source wire, an earthing conductor, or the 1st charge pulse line in order to charge the 1st bootstrap capacity.

The 2nd bootstrap capacity that one end was connected to a gate of the 1st charging transistor, and was connected to an output to which the other end was driven by the 2nd sauce or source mode output of an output transistor, Sauce is connected to an end of the 2nd bootstrap capacity in order to charge the 2nd bootstrap capacity, The 2nd charging transistor that a drain was connected to a power source wire, an earthing conductor, or the 2nd charge pulse line, and was connected to an output to which a gate was driven by the 3rd sauce or source mode output of an output transistor.

[0025]According to this composition, first by a source mode output of the 3rd output transistor (for example, it can set to a unit circuit of a beforehand stage) being impressed to a gate of the 2nd charging transistor. By the 2nd bootstrap capacity being charged, one end of the 2nd bootstrap capacity being connected to a gate of the 1st charging transistor, and an output of the 2nd output transistor

(for example, it can set to a unit circuit of the preceding paragraph) being applied to the other end. Voltage higher than before will be added to a gate of the 1st charging transistor, and gate potential of the 1st charging transistor can be made higher than the power supply voltage VDD. Thereby, the 1st bootstrap capacity can be charged at the power supply voltage VDD, and descent of charge voltages to the 1st bootstrap capacity can be prevented. Therefore, when a transmission number of stages increases, it can prevent that output pulse voltage does not decline gradually or an output pulse stops coming out at several steps or the point.

[0026]As for the 4th signal transmission circuit, it is preferred to have the 1st discharge transistor by which a drain was connected to sauce of the 1st charging transistor, and the 2nd discharge transistor by which a drain was connected to sauce of the 2nd charging transistor.

[0027]The 3rd discharge transistor connected to a terminal in which the 4th signal transmission circuit differs from a terminal to which the 1st discharge transistor of the 1st bootstrap capacity was connected, It is preferred to have the 4th discharge transistor connected to a different terminal from a terminal to which said 2nd discharge transistor of the 2nd bootstrap capacity was connected.

[0028]In this case, it is preferred that the 3rd discharge transistor and the 4th discharge transistor are the same transistors.

[0029]In a gate of the 3rd and 4th discharge transistors, it is preferred that a drive pulse is inputted. Thereby, it can discharge by being stabilized by a direct-drive pulse being added.

[0030]It is preferred that an output driven by the 1st source voltage or source voltage of an output transistor is supplied to a gate of the 2nd discharge transistor and the 3rd discharge transistor of the preceding paragraph. Thereby, the 2nd bootstrap capacity and the 1st bootstrap capacity of the preceding paragraph can be discharged simultaneously.

[0031]Thus, only by adding four discharge transistors, discharge of bootstrap capacity can be performed and this invention can be applied also to small circuitry of a scale without other external input pulses.

[0032]In the 4th signal transmission circuit, the 2nd output transistor is an output transistor in a unit circuit of the preceding paragraph, and, as for the 3rd output transistor, it is preferred that it is an output transistor in a unit circuit of a beforehand stage.

[0033]According to this composition, by using an output of a shift register, an

excessive pulse added to a gate of a charging transistor can be omitted, and circuit structure can be made small.

[0034]As for the 3rd and 4th signal transmission circuits, it is preferred that a drain is provided with a transistor for malfunction prevention connected to a gate of the 1st output transistor.

[0035]According to this composition, even when threshold voltage of an output transistor is low, malfunction can be prevented, and the wide range of threshold voltage can be taken.

[0036]As for the 3rd and 4th signal transmission circuits, it is preferred to have a transistor for malfunction prevention by which a drain was connected to a gate of the 1st output transistor, and a gate was connected to sauce of an output transistor of a beforehand stage.

[0037]According to this composition, this invention is applicable also to small circuitry of a scale without other external input pulses with having constituted so that sauce of an output transistor of a beforehand stage might be connected to a gate of a transistor for malfunction prevention.

[0038]In the 3rd and 4th signal transmission circuits, it is preferred that a power-supply-voltage pulse which enables operation of a charging transistor of a

period when pulse voltage is outputted to sauce of an output transistor of a certain stage, and the next step, and makes one charging transistor of a stage after another prohibition of operation is supplied to a drain. For example, when a charging transistor consists of NMOSes, as a power-supply-voltage pulse, "High" level voltage is supplied to a drain of a charging transistor of the next step, and "Low" level voltage is supplied to a drain of a charging transistor of a stage one after another. When a charging transistor consists of PMOSes, as a power-supply-voltage pulse, "Low" level voltage is supplied to a drain of a charging transistor of the next step, and "High" level voltage is supplied to a drain of a charging transistor of a stage one after another.

[0039]According to this composition, a transistor for malfunction prevention can be omitted and circuit structure can be reduced.

[0040]Or it is preferred that conductance of the 1st charging transistor is smaller than conductance of a transistor for malfunction prevention.

[0041]According to this composition, the positive terminal side of the 1st bootstrap capacity can be brought more close to 0V, and malfunction can be prevented more certainly.

[0042]In the 3rd and 4th signal transmission circuits, when all transistors are

NMOS transistors, earth potentials are supplied to at least one of sauce of the 1st to 4th discharge transistor, and sauce of a transistor for malfunction prevention.

[0043]Or when all transistors are NMOS transistors in the 3rd and 4th signal transmission circuits, To at least one of sauce of the 1st to 4th discharge transistor, and sauce of a transistor for malfunction prevention, voltage lower than threshold voltage of the 1st output transistor is supplied.

[0044]In the 3rd and 4th signal transmission circuits, when all transistors are PMOS transistors, power supply voltage is supplied to at least one of sauce of the 1st to 4th discharge transistor, and sauce of a transistor for malfunction prevention.

[0045]Or when all transistors are PMOS transistors in the 3rd and 4th signal transmission circuits, To at least one of sauce of the 1st to 4th discharge transistor, and sauce of a transistor for malfunction prevention, voltage higher than threshold voltage of the 1st output transistor is supplied.

[0046]By the above-mentioned composition, a charging transistor or an output transistor is stabilized and a state of OFF can be maintained.

[0047]In order to attain the aforementioned purpose, a solid state camera

concerning this invention was provided with the 3rd or 4th signal transmission circuit.

[0048]In order to attain the aforementioned purpose, a camera concerning this invention carried a solid state camera concerning this invention.

[0049]In order to attain the aforementioned purpose, a display concerning this invention was provided with the 3rd or 4th signal transmission circuit.

[0050]According to the above-mentioned composition, an effect can be demonstrated in a solid state camera and a camera which carries it which can guarantee stable operation even if it carries out voltage lowering of the circuit power source, and are applied to a portable equipment which needs to attain especially low power consumption, and a liquid crystal display.

[0051]

[Embodiment of the Invention]Hereafter, the suitable embodiment of this invention is described with reference to drawings.

[0052](A 1st embodiment) Drawing 1 is a circuit diagram showing the example of 1 composition of the signal transmission circuit concerning a 1st embodiment of this invention. The gate of the discharge transistor of the preceding paragraph is connected common to the sauce of the output transistor of the next step, and the

point that this embodiment differs from the conventional example shown in drawing 4 is one of the points that common output pulse voltage is impressed. About other composition, it is the same as the conventional example of drawing 5, and the same numerals are attached in drawing 1.

[0053]In drawing 1, if the start pulse VST is set to a logic "High" level, The 1st charging transistor T11 that charges the 1st bootstrap capacity C11 in the first rank is turned on, One [the output transistor T12 of the first rank] if the 1st bootstrap capacity C11 is charged with the power supply voltage VDD and the charge voltages of the 1st bootstrap capacity C11 exceed the threshold voltage level of the output transistor T12.

[0054]Then, when the drive pulse V1 of a logic "High" level inputs into the drain of the output transistor T12, in the gate of the output transistor T12. If the voltage of the drive pulse V1 and the potential difference of the 1st bootstrap capacity C11 both ends will be added and impressed and the gate potential of the output transistor T12 rises rather than the potential of the drive pulse V1, The drive pulse V1 is used as output pulse OUT1 from the output node N12 of the first rank.

[0055]Simultaneously, if the drive pulse V1 is outputted to the node N12, the 2nd step of 1st charging transistor T21 by which the gate was connected to the node

N12 will be turned on, One [the 2nd step of output transistor T22] if the 1st bootstrap capacity C21 is charged with the power supply voltage VDD and the charge voltages of the 1st bootstrap capacity C21 exceed the threshold voltage level of the output transistor T22.

[0056]Then, when the drive pulse V2 of a logic "High" level inputs into the drain of the output transistor T22, in the gate of the output transistor T22. If the potential of the drive pulse V2 and the potential difference of the 1st capacity C21 both ends for a bootstrap will be added and impressed and the gate potential of the output transistor T22 rises rather than the potential of the drive pulse V2, The drive pulse V2 is used as output pulse OUT2 from the 2nd step of output node N22.

[0057]Since this output pulse OUT2 is impressed common to the gate of the 1st discharge transistor T13 in the first rank, and the 2nd discharge transistor T14, When the drive pulse V2 is outputted to the 2nd step of output node N22, the electric charge of the 1st bootstrap capacity C11 both ends of the first rank will be discharged at high speed and simultaneous.

[0058]Even if the advantage of the signal transmission circuit by this embodiment accelerates a circuit power source by discharging the electric

charge of the both ends of the 1st bootstrap capacity C11 at high speed and simultaneous, stable operation is possible for it here, and a signal transmission circuit suitable for improvement in the speed can be realized.

[0059]Simultaneously, if the drive pulse V2 is outputted to the node N22, the 3rd step of 1st charging transistor T31 by which the gate was connected to the node N22 will be turned on, One [the 3rd step of output transistor T32] if the 1st bootstrap capacity C31 is charged with the power supply voltage VDD and the charge voltages of the 1st bootstrap capacity C31 exceed the threshold voltage level of the output transistor T32.

[0060]Then, when the drive pulse V1 of a logic "High" level inputs into the drain of the output transistor T32, in the gate of the output transistor T32. If the potential of the drive pulse V1 and the potential difference of the 1st capacity C31 both ends for a bootstrap will be added and impressed and the gate potential of the output transistor T32 rises rather than the potential of the drive pulse V1, The drive pulse V1 is used as output pulse OUT3 from the 3rd step of output node N32.

[0061]Since this output pulse OUT3 is impressed common to the gate of the 1st discharge transistor T23 in the 2nd step, and the 2nd discharge transistor T24,

When the drive pulse V1 is outputted to the 3rd step of output node N32, the electric charge of the 2nd step of 1st bootstrap capacity C21 both ends will be discharged at high speed and simultaneous.

[0062]By such operation being repeated, a signal transmission circuit will output an output pulse one by one further.

[0063]Although each sauce of the 1st and 2nd discharge transistors is made into earth potentials (0V), if each source voltage is a value smaller than the threshold voltage of an output transistor, the same effect will be acquired even if it is not 0V.

[0064](A 2nd embodiment) Drawing 2 is a circuit diagram showing the example of 1 composition of the signal transmission circuit concerning a 2nd embodiment of this invention. In the unit circuit after the 2nd step the point that this embodiment differs from a 1st embodiment, The 2nd bootstrap capacity (C22, C32) and the 2nd charging transistor (T25, T35) that charges the 2nd bootstrap capacity, In the 3rd discharge transistor (T26, T36) that discharges the electric charge of the both ends of the 2nd bootstrap capacity, and the unit circuit after the 3rd step, To the plus side edge child (node N31) of the 1st bootstrap capacity (C31), a drain, A gate is connected to the output node (N12) of the beforehand

stage, and the transistor for malfunction prevention (T38) with which sauce is grounded is added, The plus side edge child (the node N25, N35) of the 2nd bootstrap capacity is connected to the gate of the 1st charging transistor (T21, T31) in the own stage, It is in the point of having connected the minus side edge child (the node N12, N22) of the 2nd bootstrap capacity to the gate of the 2nd charging transistor (T25, T35) in the next step.

[0065]In drawing 2, if start pulse VST2 is set to a logic "High" level, The 1st charging transistor T11 that charges the 1st bootstrap capacity C11 in the first rank is turned on, One [the output transistor T12 of the first rank] if the 1st bootstrap capacity C11 is charged with the power supply voltage VDD and the charge voltages of the 1st bootstrap capacity C11 exceed the threshold voltage level of the output transistor T12.

[0066]If start pulse VST1 is set to a logic "High" level, the 2nd charging transistor T25 that charges the 2nd bootstrap capacity C22 in the 2nd step will be turned on, and the 2nd bootstrap capacity C22 will be charged with the power supply voltage VDD.

[0067]Then, when the drive pulse V1 of a logic "High" level inputs into the drain of the output transistor T12, in the gate of the output transistor T12. If the voltage

of the drive pulse V1 and the potential difference of the 1st bootstrap capacity C11 both ends will be added and impressed and the gate potential of the output transistor T12 rises rather than the potential of the drive pulse V1, The drive pulse V1 is used as output pulse OUT1 from the output node N12 of the first rank.

[0068]Here the advantage of the signal transmission circuit by this embodiment, In the gate of the 2nd step of 1st charging transistor T21 connected to the node N25 of the plus side edge child of the 2nd charged bootstrap capacity C22. The voltage of the drive pulse V1 and the potential difference of the 2nd bootstrap capacity C22 both ends which were outputted to the output node N12 will be added and impressed, Since it goes up rather than the power supply voltage VDD whose gate potential of the 1st charging transistor T21 is drain potential, it is in the point that the 2nd step of 1st bootstrap capacity C21 can be charged at the power supply voltage VDD.

[0069]By this, even if the 1st charging transistor T21 that charges the 2nd step of 1st capacity C21 for a bootstrap is NMOS of an enhancement type, The 1st bootstrap capacity C21 can be charged certainly at the power supply voltage VDD, and the output transistor T22 can be made one.

[0070]When the drive pulse V1 is outputted to the output node N12,

simultaneously, and the 3rd step of 2nd bootstrap capacity C32 is charged. [the 3rd step of 2nd charging transistor T35 by which the gate was connected to the output node N12]

[0071]Then, when the drive pulse V2 of a logic "High" level inputs into the drain of the output transistor T22, in the gate of the output transistor T22. If the potential of the drive pulse V2 and the potential difference of the 1st bootstrap capacity C21 both ends will be added and impressed and the gate potential of the output transistor T22 rises rather than the potential of the drive pulse V2, The drive pulse V2 is used as output pulse OUT2 from the 2nd step of output node N22.

[0072]In the gate of the 3rd step of 1st charging transistor T31 simultaneously connected to the node N35 which is a plus side edge child of the 2nd bootstrap capacity C32. The voltage of the drive pulse V2 and the potential difference of the 2nd bootstrap capacity C32 both ends which were outputted to the output node N22 will be added and impressed, One [the 3rd step of 1st bootstrap capacity C31 is certainly charged by the power supply voltage VDD, and / the output transistor T32] since the gate potential of the 1st charging transistor T31 rises rather than the power supply voltage VDD which is drain potential.

[0073]By such operation being repeated, a signal transmission circuit will output the output pulse OUT3 or subsequent ones one by one further.

[0074]Thus, in all the signal-transmission stages, the 1st bootstrap capacity can charge the power supply voltage VDD certainly, and the signal transmission circuit which can generate the output pulse of the low voltage without a voltage drop can be realized.

[0075]In order to lessen the transistor and power supply of a circuit as a means to discharge the voltage which charged bootstrap capacity, in the case of the 1st bootstrap capacity C21 in the 2nd step, The drain of the 1st discharge transistor T23 is connected to the plus side edge child of the 1st bootstrap capacity C21, The drain of the 2nd discharge transistor T24 is connected to the minus side edge child of the 1st bootstrap capacity C21, The output node N32 connected to the sauce of the 3rd step of output transistor T32 which is the next step at the gate of the 1st discharge transistor T23 and the 2nd discharge transistor T24 is connected. By this, when the drive pulse V1 is outputted to the 3rd step of output node N32, the 1st bootstrap capacity C21 in the 2nd step will be discharged.

[0076]On the other hand, in the case of the 2nd bootstrap capacity C22 in the 2nd step, The output node N22 which connected the drain of the 3rd discharge

transistor T26 to the plus side edge child of the 2nd bootstrap capacity C22, and was connected to the sauce of the 2nd step of output transistor T22 which is self at the gate of the 3rd discharge transistor T26 is connected. By this, when the drive pulse V2 is outputted to the 2nd step of output node N22, the 2nd bootstrap capacity C22 in the 2nd step will be discharged.

[0077]By this composition, only by adding three discharge transistors, the 1st and 2nd bootstrap capacity can be discharged and the small circuitry of a scale without other external input pulses can also realize the signal transmission circuit of this embodiment.

[0078]The drain was connected to the plus side edge child (node N31) of the 1st bootstrap capacity C31 in the 3rd step, the gate was connected to the output node N12 in the first rank, and the transistor T38 for malfunction prevention with which sauce was grounded is formed. One [the 1st charging transistor T31 / with the potential of the node N35 / some] when the 2nd bootstrap capacity C32 in the 3rd step is charged. And one [since the 1st bootstrap capacity C31 is charged somewhat] although the output transistors T32 are some when the threshold voltage of the output transistor T32 is low. When the drive pulse V1 is outputted to the output node N12 of the first rank at this time, the drive pulse V1

may be simultaneously outputted also to the 3rd step of output node N32.

[0079]In order to prevent outputting the drive pulse V1 to the output node N32, When the transistor T38 for malfunction prevention is formed and the drive pulse V1 is outputted to the output node N12 of the first rank, the node N31 is made into the 0V neighborhood, and the drive pulse V1 is made not to be outputted to the 3rd step of output node N32. [the transistor T38 for malfunction prevention]

[0080]At this time, the conductance of the 1st charging transistor T31 in the 3rd step by making it smaller than the conductance of the transistor T38 for malfunction prevention. The positive terminal side of the 1st bootstrap capacity C31 can be brought more close to 0V, and malfunction can be prevented more certainly.

[0081]Thus, the transistor for malfunction prevention is provided in each stage after the 3rd step, and by impressing the output pulse of the beforehand stage to the gate of the transistor for malfunction prevention, even when the threshold voltage of an output transistor is low, malfunction can be prevented, and the wide range of threshold voltage can be taken.

[0082]With having constituted so that the sauce of the output transistor of the beforehand stage might be connected to the gate of the transistor for

malfunction prevention, even when it is small circuitry of a scale without other external input pulses, the signal transmission circuit by this embodiment can be realized.

[0083]Although each sauce of the discharge transistor and the transistor for malfunction prevention is made into earth potentials (0V), if each source voltage is a value smaller than the threshold voltage of an output transistor, the same effect will be acquired even if it is not 0V.

[0084]Since DC voltage is impressed to the drain of the 1st and 2nd charging transistors as the power supply voltage VDD, a possibility that malfunction will take place occurs in it, and it is necessary in it to include the transistor for malfunction prevention but, and. Malfunction can be prevented by impressing pulse voltage to the drain of a charging transistor as the power supply voltage VDD. That is, the drain of the charging transistor of the period and the next step which output voltage has generated in the sauce of an output transistor can be used as the "High" level, and the transistor for malfunction prevention can be omitted by using one drain of the charging transistor of the stage after another as the "Low" level.

[0085]Drawing 3 is a timing chart which shows the pulse voltage of each part in

the signal transmission circuit of drawing 2 which used only NMOS. This circuit is a circuit of 3V system, and shows the case where the drive pulse V1, the voltage swing of V2, and the power supply voltage VDD are 3V. However, the voltage swing of start pulse VST2 sets the voltage swing of 5V and start pulse VST1 to 3V. Setting only the voltage swing of start pulse VST2 to 5V here, Since the high voltage from the preceding paragraph cannot be supplied only when it is the 1st charging transistor T11 of the first rank into which start pulse VST2 is inputted, When only start pulse VST2 drives the 1st charging transistor T11 by 5V [higher than 3V which is the drive pulse V1 and a voltage swing of V2], It is because the voltage drop by the 1st charging transistor T11 is prevented and charge of 3V which is the power supply voltage VDD of the 1st bootstrap capacity C11 is enabled.

[0086]In drawing 3, the voltage of start pulse VST2 rises to 5V in the time t0, One [the 1st bootstrap capacity C11 is charged via the transistor T11 by 3V which is the power supply voltage VDD, and / the output transistor T12] even when there is the threshold voltage Vt of the 1st charging transistor T11 that is NMOS of an enhancement type.

[0087]Simultaneously, the voltage of start pulse VST1 rises to 3V, and the 2nd

bootstrap capacity C22 is charged via the 2nd charging transistor T25.

[0088]Next, when the drive pulse V1 rises to 3V and inputs into the drain of the output transistor T12 in the time t1, in the gate of the output transistor T12. Since voltage HB 1 high voltage to which the voltage 3V of the drive pulse V1 and the potential difference 3V of bootstrap capacity C11 both ends were added is impressed, the drive pulse V1 of 3V amplitude will be certainly outputted as output pulse OUT1 from the output node N12.

[0089]And one [high-tension HB 25 of the node N25 connected to the plus side edge child of the 2nd bootstrap capacity C22 is simultaneously inputted into the gate of the 1st charging transistor T21, and / the transistor T21], The 1st bootstrap capacity C21 will be charged by 3V which is the power supply voltage VDD certainly.

[0090]At this time, the voltage (3 V-delta H35) in which the node N35 is lower than 3V is charged, and the same voltage also as the gate of the 1st charging transistor T31 is impressed. In this case, so that the potential of the node N31 connected to the sauce of the 1st charging transistor T31 may not become more than the threshold voltage of the 1st charging transistor T31, By and bringing the node N31 in the earth-potentials direction close, it can prevent outputting the

drive pulse V1 to the node N32 at the time t1. [the malfunction prevention transistor T38]

[0091]Similarly, also in time t2 and t3, operation of the time t1 will be repeated.

[0092]As mentioned above, in order to add the plus side edge child voltage of the 2nd bootstrap capacity to the gate of the 1st charging transistor according to this embodiment, The signal transmission circuit which can generate the output pulse of the low voltage of 3V which can charge the 1st bootstrap capacity certainly at the power supply voltage 3V, and does not have a voltage drop is realizable.

[0093]In this embodiment, although the case of the NMOS transistor was illustrated and explained, the same effect can be acquired also about the case where it is a PMOS transistor altogether.

[0094]Amplitude can be enlarged for the source voltage of an output transistor using a drive circuit, and voltage can be increased in this embodiment.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]The circuit diagram showing the example of 1 composition of the signal transmission circuit concerning a 1st embodiment of this invention

[Drawing 2]The circuit diagram showing the example of 1 composition of the signal transmission circuit concerning a 2nd embodiment of this invention

[Drawing 3]The timing chart which shows the pulse voltage of each part in the signal transmission circuit of drawing 2

[Drawing 4]The circuit diagram showing the example of 1 composition of the conventional signal transmission circuit

[Drawing 5]The timing chart which shows the pulse voltage of each part in the signal transmission circuit of drawing 4

[Description of Notations]

C11, C21, and C31 The 1st bootstrap capacity

C22 and C32 The 2nd bootstrap capacity

OUT1, OUT2, OUT3 output pulse (scanning pulse)

T11, T21, and T31 The 1st charging transistor

T25 and T35 The 2nd charging transistor

T12, T22, T32 output transistor

T13, T23, and T33 1st discharge transistor

T14, T24, and T34 2nd discharge transistor

T26 and T36 3rd discharge transistor

T38 Transistor for malfunction prevention

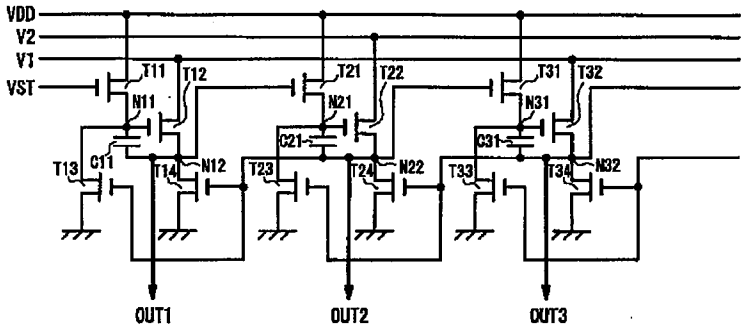
V1, V2 drive pulse

VDD Power supply voltage

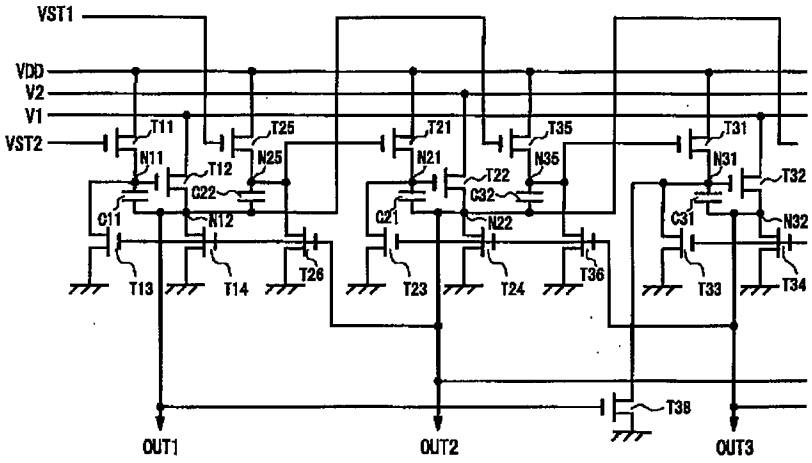
VST, VST1, and VST2 Start pulse

DRAWINGS

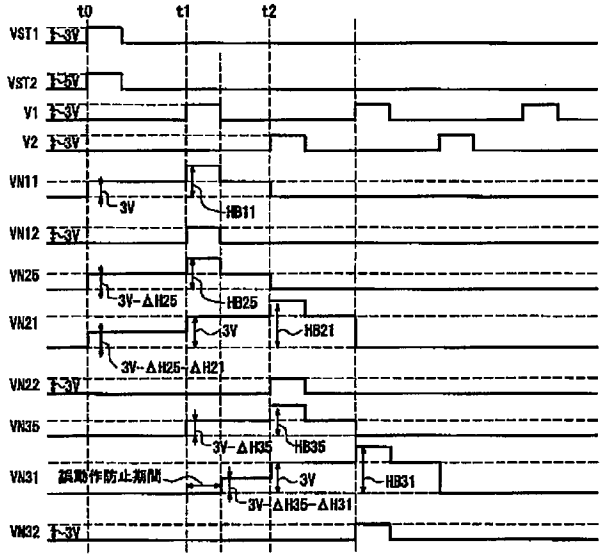
[Drawing 1]



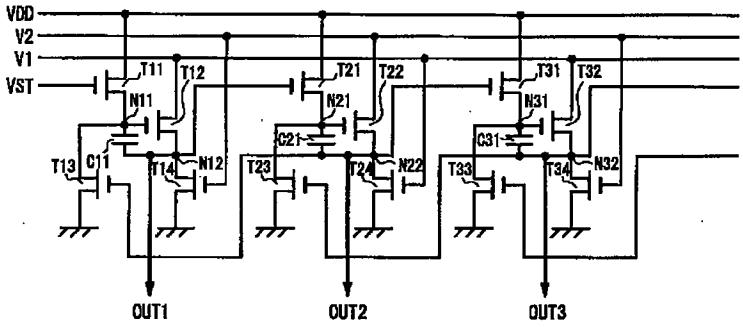
[Drawing 2]



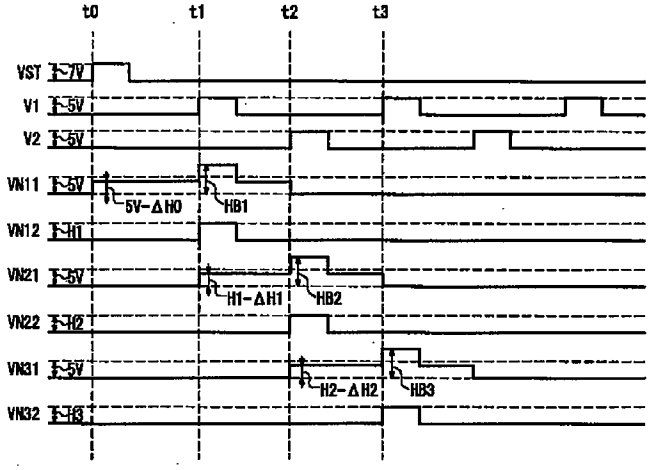
[Drawing 3]



[Drawing 4]


VDD
V2
V1
VST
T11
T12
N11
T13
C11
T14
N12
T21
T22
N21
C21
T23
T24
N22
T31
T32
N31
C31
T33
T34
N32
OUT1
OUT2
OUT3

[Drawing 5]


t0
t1
t2
t3
VST
V1
V2
VN11
VN12
VN21
VN22
VN31
VN32
5V-ΔH0
HB1
H1-ΔH1
HB2
H2-ΔH2
HB3